Application No. 10/549,784
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Response to Notification dated 5/8/06

Patent Claims

1. A semiconductor configuration for controlling a current (I) comprising at least:

a) a first semiconductor region (2) of a first conductivity type,

b) a current path running at least partially within the first semiconductor region (2),

d) a channel region (22),

C1) being part of the first semiconductor region (2),

c2) having a basic doping, and

c3) within which the current (I) can be influenced by means of at least one depletion zone (23, 24),

characterized in that

c4) the channel region (22) comprises a channel conduction region (225) intended for carrying current and having the first conductivity type and a higher doping compared with the basic doping.

2. The semiconductor configuration as claimed in claim 1, in which the current path essentially runs in the vertical direction.

3. The semiconductor configuration as claimed in claim 1 or 2, in which the channel region (22) is formed as a lateral channel region.

4. The semiconductor configuration as claimed in one of the preceding claims, which is formed as a field effect transistor, in particular as a junction field effect transistor.

5. The semiconductor configuration as claimed in one of the preceding claims, in which silicon carbide is provided as semiconductor material.

6. The semiconductor configuration as claimed in one of the preceding claims, in which an island region (3) of a second conductivity type being opposite to the first conductivity type is arranged, the island region being at least partially buried within the first semiconductor region (2).

7. The semiconductor configuration as claimed in one of the preceding claims, in which at least 80%, in particular at least 90% of the total charge of the first conductivity type present within the channel region (22) is situated within the channel conduction region (225).

8. The semiconductor configuration as claimed in one of the preceding claims, in which at least one channel compensation region (226) is arranged within the channel conduction region (225).

9. The semiconductor configuration as claimed in claim 8, in which the at least one channel compensation region (226) has a second conductivity type opposite to the first conductivity type.

10. The semiconductor configuration as claimed in claim 8 or 9, in which the at least one channel compensation region (226) has a higher dopant concentration than the channel conduction region (225).

11. The semiconductor configuration as claimed in one of claims 8 to 10, in which the total charge of the first conductivity type introduced into the channel conduction region (225) is approximately equal in magnitude to the total charge of the second conductivity type introduced into the one channel compensation region (226) or, in the case of a plurality of channel compensation regions (226), into all of the channel compensation regions (226).

12. The semiconductor configuration as claimed in one of the preceding claims, in which the channel region (22) is arranged in an epitaxial layer (262).

13. The semiconductor configuration as claimed in claim 12, in which the doping of the epitaxial layer (262) is equal to the basic doping.

14. The semiconductor configuration as claimed in one of the preceding claims, in which the first semiconductor region (2) comprises two epitaxial layers (261, 262) having an essentially identical doping.

15. The semiconductor configuration as claimed in one of the preceding claims, in which the first semiconductor region (2) is arranged on a substrate (28) of a second conduction type, opposite to the first conductivity type, and the current path also runs through the substrate (28).

16. The semiconductor configuration as claimed in claim 15, in which an island region (3) of the second conductivity type is arranged, the island region being at least partially buried within the first semiconductor region (2), and at least on a side of the island region (3) that faces the substrate (28), a shielding region (31) of the first conductivity type is

arranged between the island region (3) and the first semiconductor region (2).

17. A method for producing a semiconductor configuration for controlling a current (I), in which at least
a) a semiconductor substrate (27) is provided,
b) an epitaxial layer (262) with a basic doping is applied to the semiconductor substrate (27), the epitaxial layer (262) comprising a channel region (22), within which the current (I) can be influenced, and
c) a channel conduction region (225) intended for carrying current and having a higher doping compared with the basic doping is implanted into the epitaxial layer (262) at least in the region of the channel region (22).

18. The method as claimed in claim 17, in which a further epitaxial layer (261) essentially having the basic doping is applied to the semiconductor substrate (27), the further epitaxial layer (261) being arranged between the semiconductor substrate (27) and the epitaxial layer (262) comprising the channel conduction region (225), and the two epitaxial layers (261, 262) being applied to the semiconductor substrate (27) progressively and one above the other.